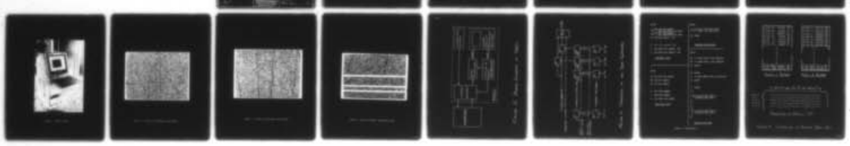
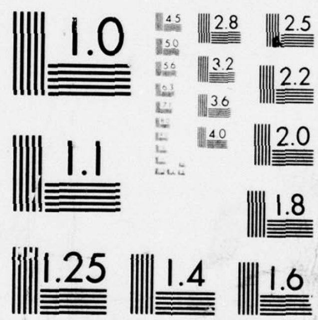
AD-A067 389   NAVAL UNDERSEA WARFARE CENTER SAN DIEGO CALIF   F/G 17/1
FUNCTIONAL DESCRIPTION OF A PASSIVE SONAR DISPLAY SIMULATOR.(U)
NOV 68 M A KUHL
UNCLASSIFIED   NUWC-TN-204   NL

| OF |
AD
A0 67389



END
DATE
FILMED
6 --79
DDC



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

LEVEL II

HAMMOND

OOVI LIBRARY COPY

NUWC TN 204

OOVICIJSM
BI lib

NAVAL UNDERSEA WARFARE CENTER

(11) NOVEMBER 1968

(12) 20p.

(14) NUWC-TN-204

MOST Project -3

(9) Technical notes

(6)

FUNCTIONAL DESCRIPTION OF A PASSIVE SONAR DISPLAY SIMULATOR.

(10) by M. A. Kuhl

San Diego, California

(16) SUBPROJECT NO. S23-26

TASK NO. 8553/8668

TN-204

002042

DISTRIBUTION STATEMENT

~~This document is subject to special export controls and each transmittal to foreign governments or foreign nationals may be made only with prior approval of the Naval Undersea Warfare Center, San Diego, Calif. 92132.~~

403 023

002042
gp-9

FOREWORD

This technical note describes a portion of the work done in Code D606 for the New Submarine Sonar/Fire Control Project Office. The information contained herein is considered to be useful to various groups within the Naval Undersea Warfare Center. Only limited distribution outside the Center is contemplated.

Among numerous persons who assisted in this development, the author is particularly indebted to J. A. Hardin, Jr., who did much of the check-out work, and to R. E. Domb, who prepared computer programs used to test all phases of equipment operation.

CONTENTS

FIGURES

INTRODUCTION

A computer-driven Passive Display Simulator (PADS) has been developed as a tool for experimental studies related to passive sonar displays. The simulator consists of an operator's console at which bearing/time data are presented in rectangular format on a CRT. Console-to-computer communication is accomplished by means of a numerical entry device. This technical note describes the simulator itself; other publications will discuss experimental work accomplished using PADS. A picture of PADS is provided as Figure 1.

Fleet sonar systems employ paper recorders for display of passive data. Early experimental work with CRT presentation of bearing/time information has been reported by Magaraci (1)*. TRACOR Incorporated (2,3) has developed a color display simulator and used it to study passive detection.

Hardware components comprising PADS are nearly all of industrial quality and were obtained at a cost of about $5000. Major items include: (1) a high-resolution, closed-circuit television monitor; (2) 43 industrial, integrated-circuit logic cards; (3) 30 militarized, discrete-component cards; (4) 2 power supplies; and (5) a console-type equipment cabinet.

The body of material which follows provides: (1) descriptions of display formats available on PADS; (2) explanations of functions performed by hardware block comprising PADS; (3) additional information needed in doing computer programming for PADS; and (4) a brief description of documents containing detailed design information.

DISPLAY FORMATS

The display area available on PADS measures approximately 9 inches horizontally by 7 inches vertically and is centered on the face of a 17-inch (diagonal

---

*See references at end of text.

measurement) CRT. A raster consisting of exactly 768 horizontal lines is scanned. The maximum number of segments into which any horizontal line can be divided is 90, and the 90-segment capability is available only when brightness levels displayed are limited to on/off (1-bit mode). The limit on number of segments per line is 45 when the option of displaying at 3 visible brightness levels plus off (2-bit mode) is chosen. Simple calculations show that the total number of discrete line segments available on the raster is 69,120 when on/off brightness is selected and 34,560 when multi-level brightness is chosen. Brightness content of the data displayed is controlled entirely by the computer.

Figures 2 and 3 illustrate the maximum display capability available in each of the brightness-level modes. Figure 4 shows a display format in which "bands" of bearing/time data are presented. Blanking of lines between bands is achieved by computer programming.

HARDWARE FUNCTIONS

Hardware comprising PADS can be divided into five major functional blocks as illustrated in Figure 5. The blocks are: (1) closed-circuit television monitor, which receives video and synchronizing signals and produces a CRT display; (2) timing and sync generator, where all timing originates and the TV sync signal is generated; (3) data shuffler, in which computer output words are converted to video for display; (4) operator entry, which allows an operator to enter data to the computer; and (5) input/output, which controls communication with the computer. Each functional block is discussed in more detail below.

Closed-Circuit Television Monitor

The closed-circuit television monitor is an industrial, electron-tube type which features 945-line scanning, P4 phosphor, and 30 MHz video channel. The usual line-up of controls is available on the monitor; most-used controls are

mounted behind a hinged panel at the front of the set. Raster width on the CRT has been reduced by means of wiring changes at the flyback transformer.

The television monitor employs interlaced scanning which minimizes the frame rate required to prevent flicker. A complete frame is painted on the CRT 30 times per second and consists of 2 interlaced fields.

In addition to power, video and synchronizing signals are inputs to the monitor. The video signal, which contains brightness information, is amplified by the monitor and applied to the cathode of the CRT. Horizontal and vertical deflection circuits in the monitor are controlled by the synchronizing signal so that raster scanning occurs in precise synchronism with the arrival of brightness data.

Timing and Synchronization

Timing within PADS is derived from an internal, 3.402 MHz crystal clock. The basic clock period (.294 μs) is the time allocated to painting a single, 1-bit line segment on the face of the CRT. Timing for display of data in the 2-bit mode is obtained by dividing the clock frequency by 2. A modulus-15 ring counter and a toggle flip-flop divide the clock frequency by 30 and provide timing needed to convert 30-bit computer words into video. A modulus-945 ripple counter driven at 56,700 kHz (clock divided by 60) provides timing used to generate the TV synchronizing signal.

Digital circuit cards are used to generate the pulse train that is standard for television synchronization in the United States. The 3 types of pulses generated and their widths are: (1) equalizing pulse, 1.4 μs; (2) horizontal sync pulse, 2.6 μs and (3) vertical sync pulse, 15 μs. Adjustable one-shot multivibrators are used to generate the pulses. Gating on the modulus-945 ripple counter serves to control formation of the pulse train.

Blanking pulses, as such, are not generated in PADS. Instead, precisely-controlled blanking is obtained by introducing all-zero words into data registers during horizontal and vertical retrace periods. Timing associated with the scanning of a single horizontal line is such that data contained in 3 computer words are painted during 3/4 of the scan period and an all-zero word blanks the CRT during the remaining 1/4 of the period (which includes horizontal retrace). Of the 945 lines scanned during a complete frame, exactly 177 lines are blanked entirely by introduction of all-zero words. The 177 blanked lines cover the vertical retrace periods between fields.

<u>Data Shuffler</u>

The data shuffler comprises the large quantity of circuit cards required to store 30-bit data words as received from the computer and to convert them to video. Operations performed are illustrated in Figure 6.

Two registers of flip-flops are used in the data shuffler. The storage register accepts a data word on command from the computer and stores it until the time for its entry into the video stream. It is then parallel-shifted into the serializing register where 29 serial shifts follow immediately. While serial shifts are taking place in the serializing register, the storage register is cleared and accepts the next data word from the computer. The storage register makes it possible for the data shuffler to receive data words at irregular intervals from the computer and still supply video in precise synchronism with the TV sweep.

Two flip-flops are driven by the serializing register and provide inputs to the digital-to-analog converter (DAC) card which outputs video. When 1-bit brightness data are being presented, only one of the 2 flip-flops drives the DAC, the clock rate to the flip-flops is maximum ($T = .294\ \mu s$), and 30 line

segments per computer word appear on the display. When 2-bit brightness data are being presented, the 2 flip-flops carry more- and less-significant bits, the clock rate to the flip-flops is halved ($T = .588\ \mu s$), and 15 line segments per computer word appear on the display.

Operator Entry

PADS is equipped with a 2-digit decimal thumbwheel device and an ENTER button. In typical operation, the operator dials a number, then presses the ENTER button which alerts the computer that some action (specified by the numerical setting) is desired. The selected number is transferred to the computer in BCD form.

Input/Output

Input/output functions in PADS involve communication with the fast interface of a UNIVAC 1230 or CP-642B computer. UNIVAC circuit cards (drivers and input amplifiers) used at PADS' end of the computer input/output cables are identical to cards used in the 1230. In PADS, most UNIVAC cards are connected to level-shifter cards which convert to and from logic levels of the industrial line of circuit cards.

Computer input words are transferred from PADS to the 1230 in the normal input sequence. PADS raises the input data request line after scanning each field and informs the computer: (1) whether the first or second field has just been scanned; (2) the reading on the numerical entry device; and (3) whether or not the ENTER button is depressed. The rate at which computer input words are transferred is fixed at one word per field which corresponds to an input data rate of 60 words per second.

Data words (which specify the information displayed on the face of the CRT) are transferred from computer to PADS in the normal output sequence. Raising

of the output data request (ODR) line by PADS is timed to make data available at appropriate times during scanning. Since 3 data words are presented on a single horizontal line and since 768 lines are refreshed 30 times per second, the computer output data rate is 69,120 words per second. The most severe test of the computer's ability to respond promptly to ODR's occurs as a line is being painted across the face of the CRT. The spacing between ODR's during this brief period is 8.8 μs, which corresponds to a computer output data rate of 117,000 words per second. Painting on the CRT is interrupted for 8.8 μs during horizontal retrace and for 3.1 ms during vertical retrace. During these periods, no ODR's are initiated by PADS.

A third type of communication between computer and PADS takes place when the computer directs PADS to switch from 1-bit to 2-bit brightness mode or vice versa. This is done by means of an external function word. PADS examines only bit 29 of the external function word in order to determine which mode is desired.

PROGRAMMING REQUIREMENTS

Part of the information needed in order to do computer programming for PADS is a knowledge of the basic hardware functions as described in the previous section. Additional information provided in this section includes: (1) details of word formats; (2) requirements imposed by interlaced scanning; and (3) use of the computer's real-time clock.

Word Formats

The 4 word formats used are illustrated in Figure 7. With respect to the 2-bit brightness data word, binary 11 produces the brightest line segment, binary 10 is next brightest, etc. In the case of 1-bit brightness, 1 is bright and 0 is blanked.

Handling of Interlace

Lines seen on the face of the CRT can be numbered, top to bottom, 0 through

767. Because scanning is interlaced, even-numbered lines, 0 through 766 are scanned during one top-to-bottom pass (field 1) and odd-numbered lines, 1 through 767, are scanned during a second pass (field 2). An obvious way to organize data to be displayed is to designate field 1 and field 2 buffer areas in the computer as illustrated in Figure 8. The computer input word should be examined in the computer to insure that field 1 data are transferred to PADS following receipt of the indication (bit 29 = 1) that field 2 has just been scanned.

Real-Time Clock

Because of its high priority on access to memory, the computer's real-time clock occasionally prohibits prompt response to an ODR from PADS. PADS deals with this situation by dropping the ODR and introducing an all-zero data word into its storage register. The result is that blanked areas, corresponding to single computer words, appear more-or-less randomly on PADS' CRT whenever the computer's real-time clock is in operation. A convenient solution to the problem is to switch off the real-time clock and use computer input word arrivals (spaced 16.7 ms) to keep track of real time.

ADDITIONAL DOCUMENTATION

The design and fabrication of PADS involved reference to and generation of quantities of documentation. Since the contents of this memorandum have been limited mostly to general information, a few items of related documentation, in which more detailed design information is available, will be described very briefly.

Information needed to operate and maintain the closed-circuit television monitor is contained in a manual supplied by the manufacturer. Seven design sketches, mostly in logic diagram form, document all functions and interconnections of UNIVAC and industrial circuit cards. Detailed information on circuit cards is available from a few pages of the 1230 maintenance manual, in the case of the

UNIVAC cards, and from an excellent design manual, in the case of the industrial cards. Two other important items of documentation are standard sync generator waveforms for TV published by the EIA and UNIVAC's publication on input/output design characteristics for UNIVAC military computers.

REFERENCES

(1) U. S. Navy Underwater Sound Laboratory Technical Memorandum Serial Number 921-019-63, Report on Initial DIMUS Sea Test, by A. F. Magaraci, CONFIDENTIAL, 30 April 1963

(2) TRACOR Document Number 67-473-U, Design and Instrumentation of a Color Display for Sonar Information, by W. J. Fontenote and A. C. Ward, 15 August 1967

(3) TRACOR Document Number 68-766-U, Summary Report on the Assessment of Color as a Sonar Display Parameter, 25 June 1968

Figure 1. Picture of PADS.

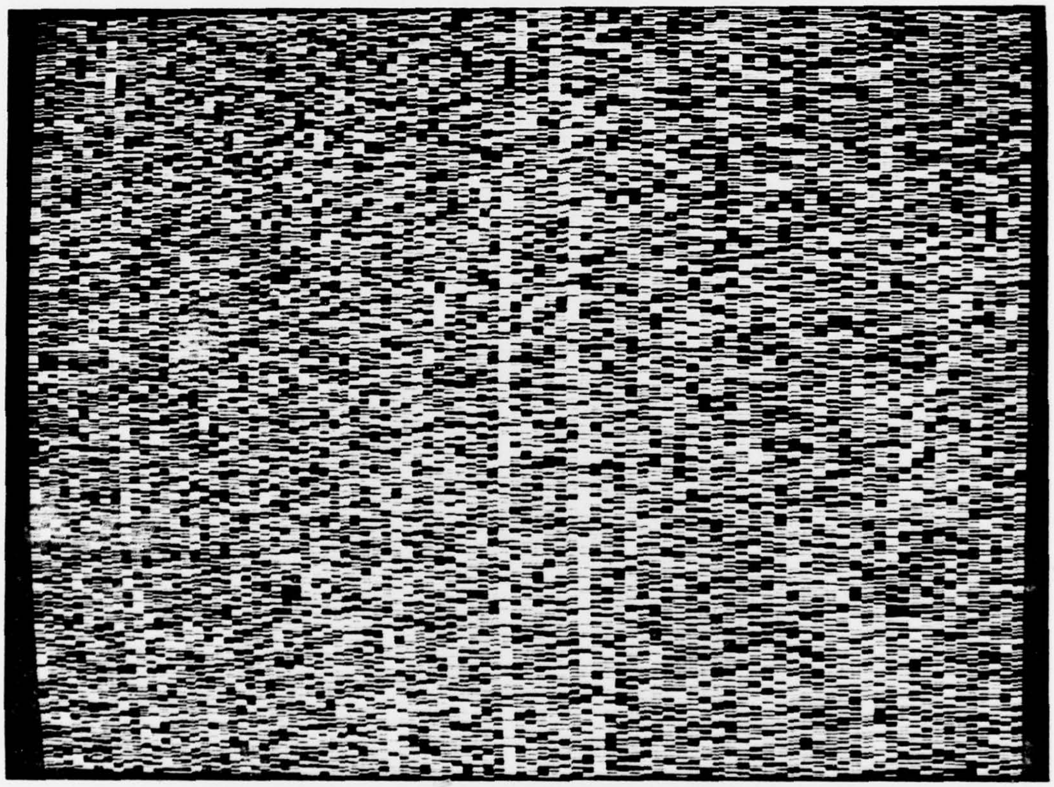


Figure 2. 768-Line by 90-Segment, 1-Bit Display.

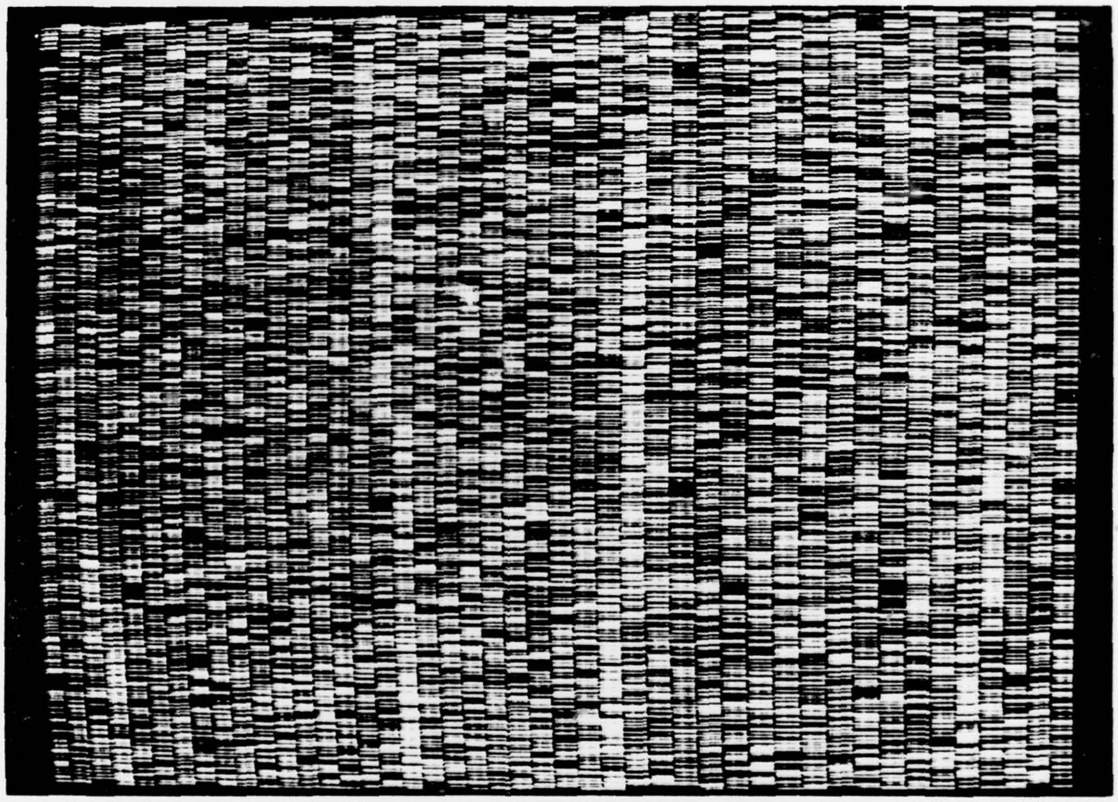


Figure 3. 768-Line by 45-Segment, 2-Bit Display.

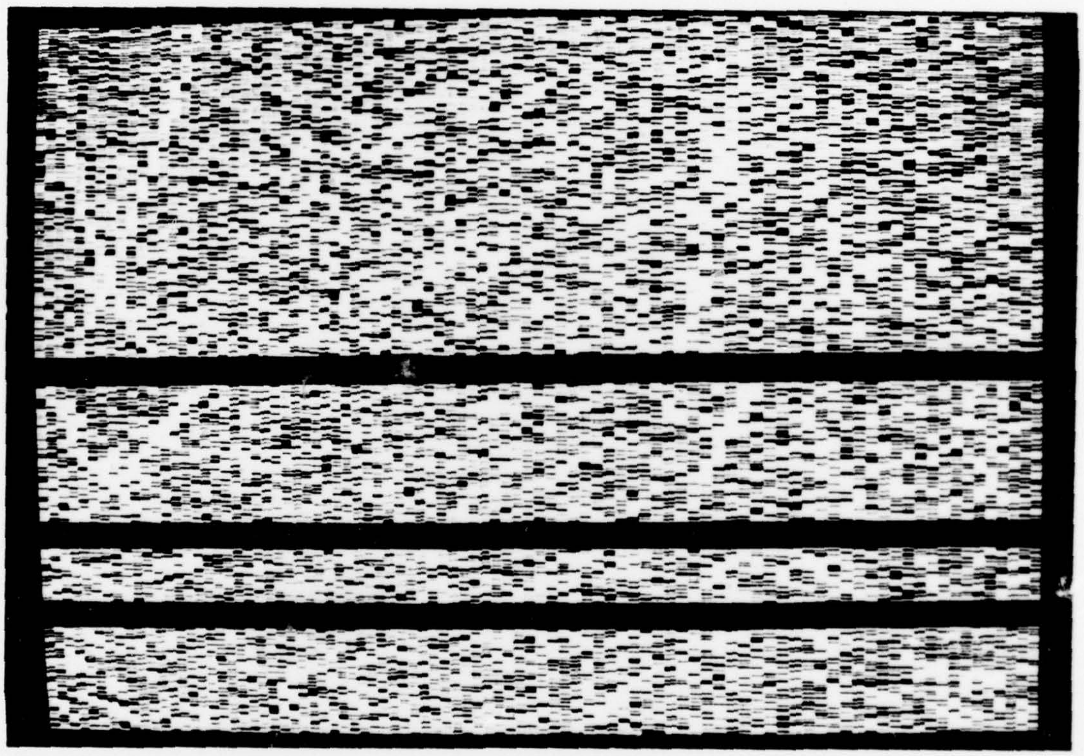


Figure 4. Display of Bands of Bearing/Time Data.

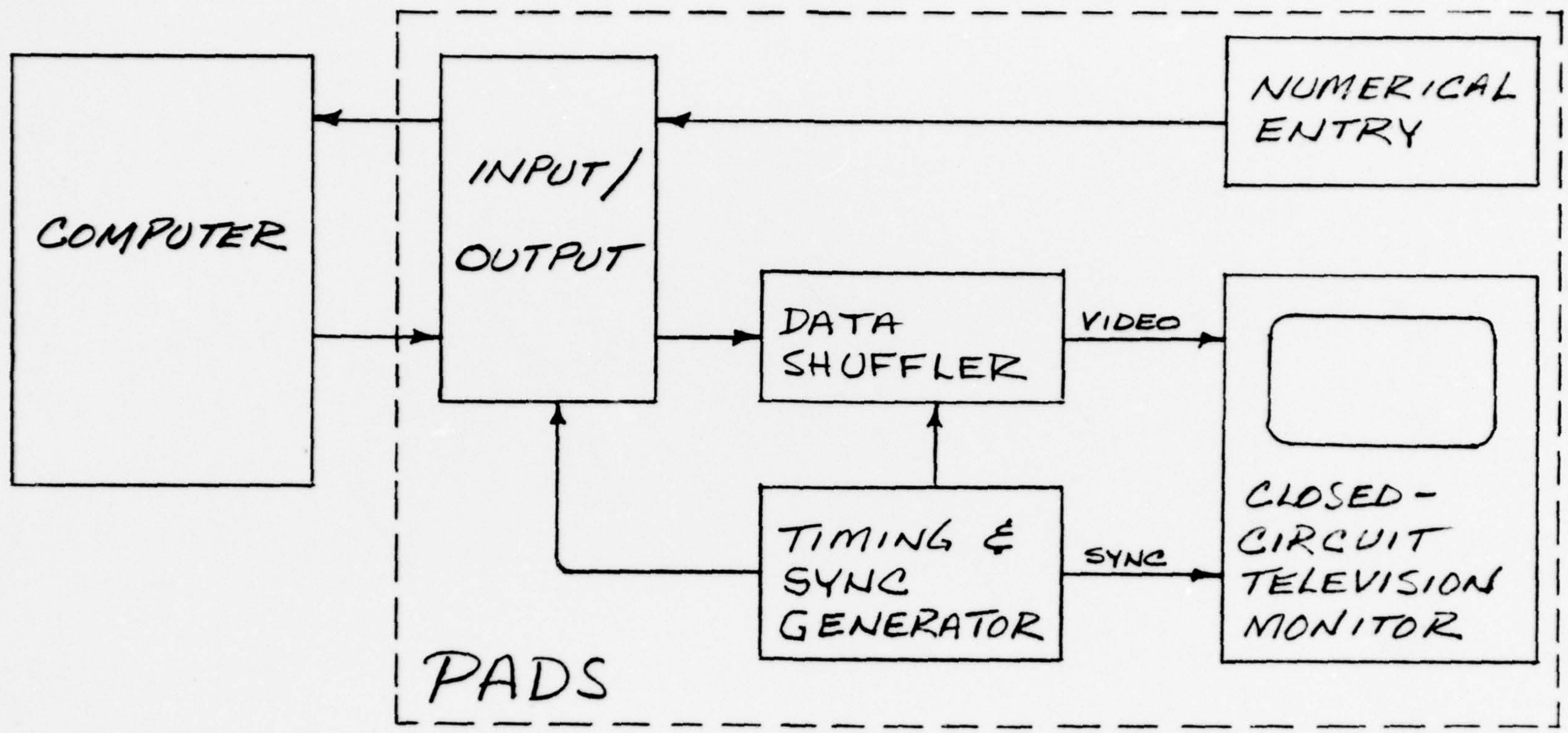


FIGURE 5. BLOCK DIAGRAM OF PADS.

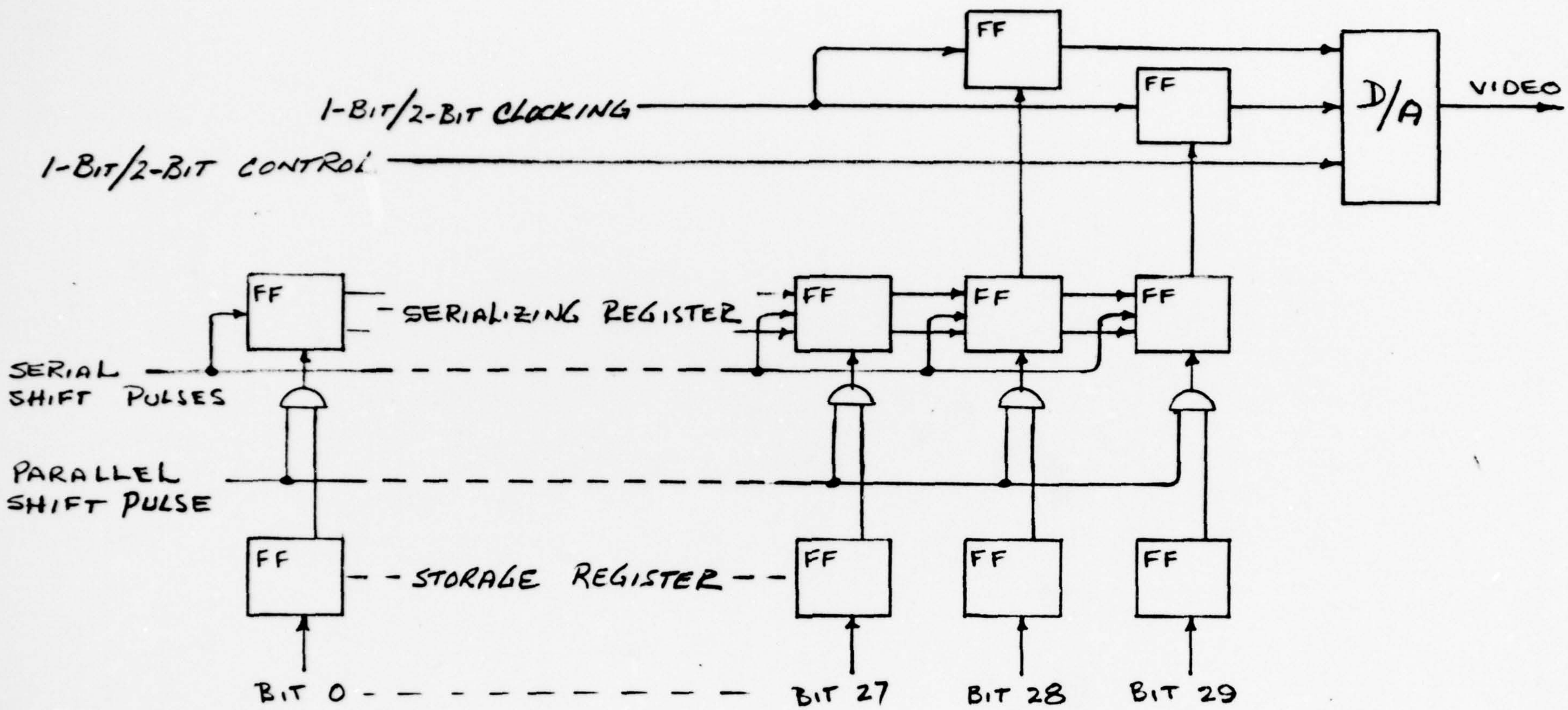


FIGURE 6. OPERATION OF THE DATA SHUFFLER.

Bit #

29 far left line segment - more significant bit (MSB)

28 far left line segment - less significant bit (LSB)

27 2nd line segment - MSB

. .

. .

. .

2 14th line segment - LSB

1 far right line segment - MSB

0 far right line segment - LSB

Data Word, 2-Bit

Bit #

29 far left line segment

28 2nd line segment

27 3rd line segment

. .

. .

. .

2 28th line segment

1 29th line segment

0 far right line segment

Data Word, 1-Bit

Bit #

29 "1" means 2-bit data follow
"0" means 1-bit data follow

28 unused

. .

. .

External Function Word

Bit #

29 "1" means field 2 just completed

28 "1" means field 1 just completed

27 unused

. .

. .

16 unused

15 "1" means ENTER button is depressed

14 unused

. .

. .

8 unused

7, 6, 5, 4 more significant digit of numerical entry (BCD)

3, 2, 1, 0 less significant digit of numerical entry (BCD)

Computer Input Word

Figure 7. Word Formats.

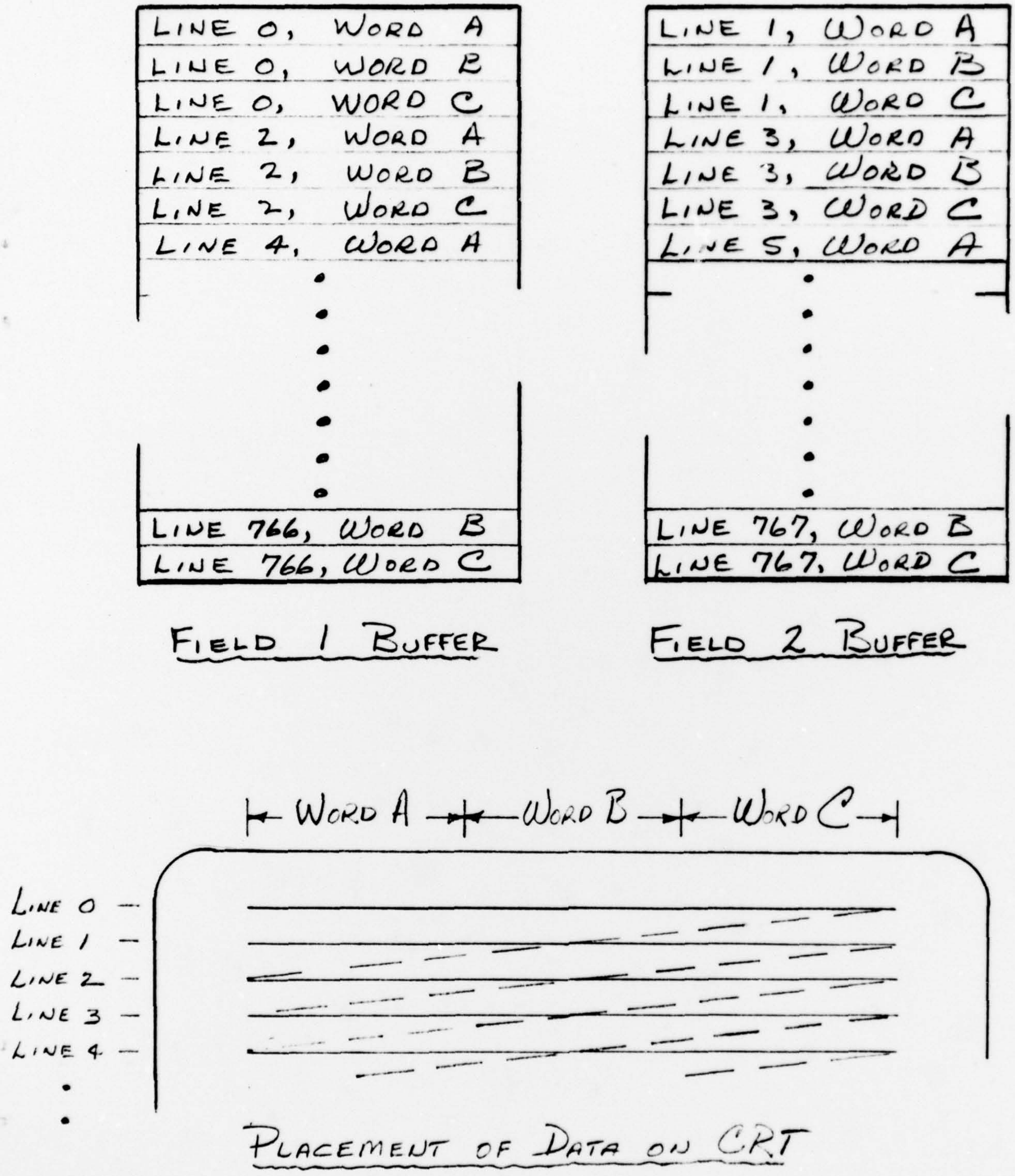


FIGURE 8. INTERLACING OF COMPUTER OUTPUT DATA.